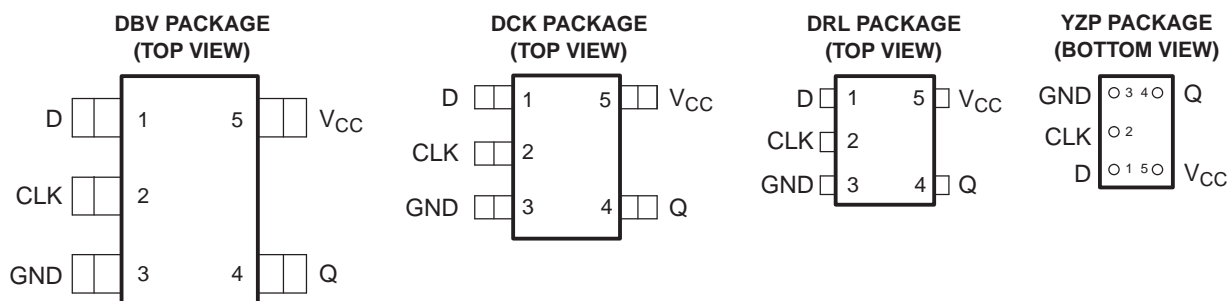


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Low Static-Power Consumption;
 $I_{CC} = 0.9 \mu\text{A Max}$
- Low Dynamic-Power Consumption;
 $C_{pd} = 3 \text{ pF Typ at } 3.3 \text{ V}$
- Low Input Capacitance;
 $C_i = 1.5 \text{ pF Typ}$
- Low Noise – Overshoot and Undershoot
<10% of V_{CC}
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys} = 250 \text{ mV Typ at } 3.3 \text{ V}$)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 3.6 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds $\pm 5000 \text{ V}$ With Human-Body Model



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

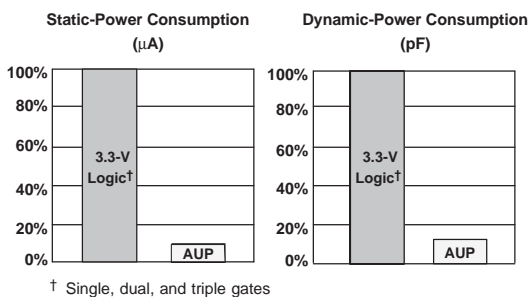


Figure 1. AUP – The Lowest-Power Family

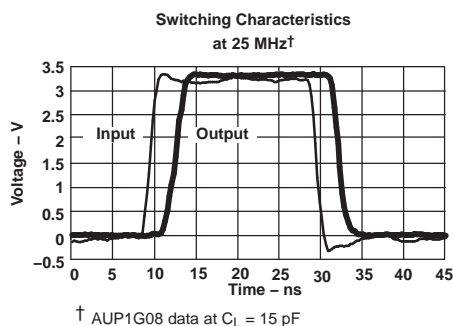


Figure 2. Excellent Signal Integrity



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUP1G79 LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES592D–JULY 2004–REVISED DECEMBER 2007

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

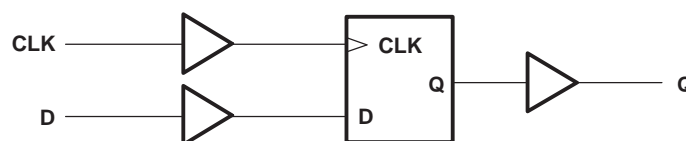
T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G79YZPR	_ _ HW _
		Reel of 250	SN74AUP1G79DBVT	H79_
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G79DBVR	H79_
		Reel of 250	SN74AUP1G79DBVT	H79_
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G79DCKR	HW_
		Reel of 250	SN74AUP1G79DCKT	HW_
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G79DRLR	HW_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L or H	X	Q ₀

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	4.6	V
V_I	Input voltage range ⁽²⁾	–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$	–50	mA
I_O	Continuous output current		±20	mA
	Continuous current through V_{CC} or GND		±50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	206	°C/W
		DCK package	252	
		DRL package	142	
		YZP package	132	
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUP1G79

LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES592D–JULY 2004–REVISED DECEMBER 2007

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.9	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
$I_{OH}^{(2)}$	High-level output current	$V_{CC} = 0.8\text{ V}$	–20	mA
		$V_{CC} = 1.1\text{ V}$	–1.1	
		$V_{CC} = 1.4\text{ V}$	–1.7	
		$V_{CC} = 1.65\text{ V}$	–1.9	
		$V_{CC} = 2.3\text{ V}$	–3.1	
		$V_{CC} = 3\text{ V}$	–4	
$I_{OL}^{(2)}$	Low-level output current	$V_{CC} = 0.8\text{ V}$	20	mA
		$V_{CC} = 1.1\text{ V}$	1.1	
		$V_{CC} = 1.4\text{ V}$	1.7	
		$V_{CC} = 1.65\text{ V}$	1.9	
		$V_{CC} = 2.3\text{ V}$	3.1	
		$V_{CC} = 3\text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$	200	ns/V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Defined by the signal integrity requirements and design-goal priorities

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = –1.7 mA	1.4 V	1.11			1.03		
	I _{OH} = –1.9 mA	1.65 V	1.32			1.3		
	I _{OH} = –2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = –3.1 mA		1.9			1.85		
	I _{OH} = –2.7 mA	3 V	2.72			2.67		
	I _{OH} = –4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V				0.1		V
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
	I _{OL} = 1.7 mA	1.4 V	0.31			0.37		
	I _{OL} = 1.9 mA	1.65 V	0.31			0.35		
	I _{OL} = 2.3 mA	2.3 V	0.31			0.33		
	I _{OL} = 3.1 mA		0.44			0.45		
	I _{OL} = 2.7 mA	3 V	0.31			0.33		
	I _{OL} = 4 mA		0.44			0.45		
I _I	D or CLK input V _I = GND to 3.6 V	0 V to 3.6 V				0.1		μA
I _{off}	V _I or V _O = 0 V to 3.6 V	0 V				0.2		μA
ΔI _{of} _f	V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V				0.2		μA
I _{CC}	V _I = GND or V _{CC} to 3.6 V, I _O = 0	0.8 V to 3.6 V				0.5		μA
ΔI _c _c	V _I = V _{CC} – 0.6 V, ⁽¹⁾ I _O = 0	3.3 V				40		μA
C _i	V _I = V _{CC} or GND	0 V				1.5		pF
		3.6 V				1.5		
C _o	V _O = GND	0 V				3		pF

(1) One-input switching

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LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES592D–JULY 2004–REVISED DECEMBER 2007

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

		V _{CC}	T _A = 25°C	T _A = –40°C to 85°C		UNIT
			TYP	MIN	MAX	
f _{clock}	Clock frequency	0.8 V		20		MHz
		1.2 V ± 0.1 V		80		
		1.5 V ± 0.1 V		100		
		1.8 V ± 0.15 V		140		
		2.5 V ± 0.2 V		210		
		3.3 V ± 0.3 V		260		
t _w	Pulse duration, CLK high or low	0.8 V		4.8		ns
		1.2 V ± 0.1 V		2.2		
		1.5 V ± 0.1 V		1.5		
		1.8 V ± 0.15 V		1.6		
		2.5 V ± 0.2 V		1.7		
		3.3 V ± 0.3 V		1.9		
t _{su}	Data high	0.8 V	2.9	4.2		ns
		1.2 V ± 0.1 V		1.4		
		1.5 V ± 0.1 V		1		
		1.8 V ± 0.15 V		0.9		
		2.5 V ± 0.2 V		0.7		
		3.3 V ± 0.3 V		0.6		
	Data low	0.8 V	3.5	5.3		
		1.2 V ± 0.1 V		1.8		
		1.5 V ± 0.1 V		1.2		
		1.8 V ± 0.15 V		1.1		
		2.5 V ± 0.2 V		1		
		3.3 V ± 0.3 V		1		
t _h	Hold time, data after CLK↑	0.8 V	0	0		ns
		1.2 V ± 0.1 V		0		
		1.5 V ± 0.1 V		0		
		1.8 V ± 0.15 V		0		
		2.5 V ± 0.2 V		0		
		3.3 V ± 0.3 V		0		

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 5 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V	93			90		MHz
			$1.2 \text{ V} \pm 0.1 \text{ V}$	199			220		
			$1.5 \text{ V} \pm 0.1 \text{ V}$	250			230		
			$1.8 \text{ V} \pm 0.15 \text{ V}$	271			240		
			$2.5 \text{ V} \pm 0.2 \text{ V}$	280			250		
			$3.3 \text{ V} \pm 0.3 \text{ V}$	280			260		
t_{pd}	CLK	Q	0.8 V	15.9					ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.7	6.9	11	2.6	13.1	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3	4.8	7.6	2	8.8	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.4	3.8	6.1	1.5	7.1	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.8	2.7	4.4	1.1	5	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	2.1	3.6	0.9	4	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V	62			50		MHz
			$1.2 \text{ V} \pm 0.1 \text{ V}$	147			160		
			$1.5 \text{ V} \pm 0.1 \text{ V}$	189			200		
			$1.8 \text{ V} \pm 0.15 \text{ V}$	180			240		
			$2.5 \text{ V} \pm 0.2 \text{ V}$	260			250		
			$3.3 \text{ V} \pm 0.3 \text{ V}$	280			260		
t_{pd}	CLK	Q	0.8 V	18					ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.3	7.8	12.3	3.2	14.4	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3.5	5.5	8.4	2.5	9.8	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.8	4.4	6.8	1.9	8	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.2	3.2	5	1.5	5.7	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.8	2.6	4.1	1.3	4.5	

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LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES592D–JULY 2004–REVISED DECEMBER 2007

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V	48			30		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	112			120		
			$1.5\text{ V} \pm 0.1\text{ V}$	151			160		
			$1.8\text{ V} \pm 0.15\text{ V}$	194			220		
			$2.5\text{ V} \pm 0.2\text{ V}$	248			250		
			$3.3\text{ V} \pm 0.3\text{ V}$	280			260		
t_{pd}	CLK	Q	0.8 V	20.3					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	5	8.7	13.6	3.9	15.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	4.1	6.3	9.3	3.1	10.7	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.3	4	7.6	2.4	8.7	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.6	3.6	5.5	1.9	6.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.2	3	4.5	1.6	5	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

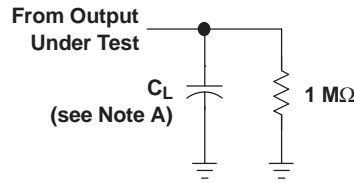
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V	24			20		MHz
			$1.2\text{ V} \pm 0.1\text{ V}$	72			80		
			$1.5\text{ V} \pm 0.1\text{ V}$	100			100		
			$1.8\text{ V} \pm 0.15\text{ V}$	127			140		
			$2.5\text{ V} \pm 0.2\text{ V}$	185			210		
			$3.3\text{ V} \pm 0.3\text{ V}$	266			260		
t_{pd}	CLK	Q	0.8 V	27.2					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	7	11.5	17.3	5.9	24	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.7	8.3	11.8	4.6	15.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.7	6.7	9.6	3.8	13	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.7	4.9	7	2.9	9	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.2	4.1	5.8	2.6	7.2	

Operating Characteristics

$T_A = 25^\circ\text{C}$

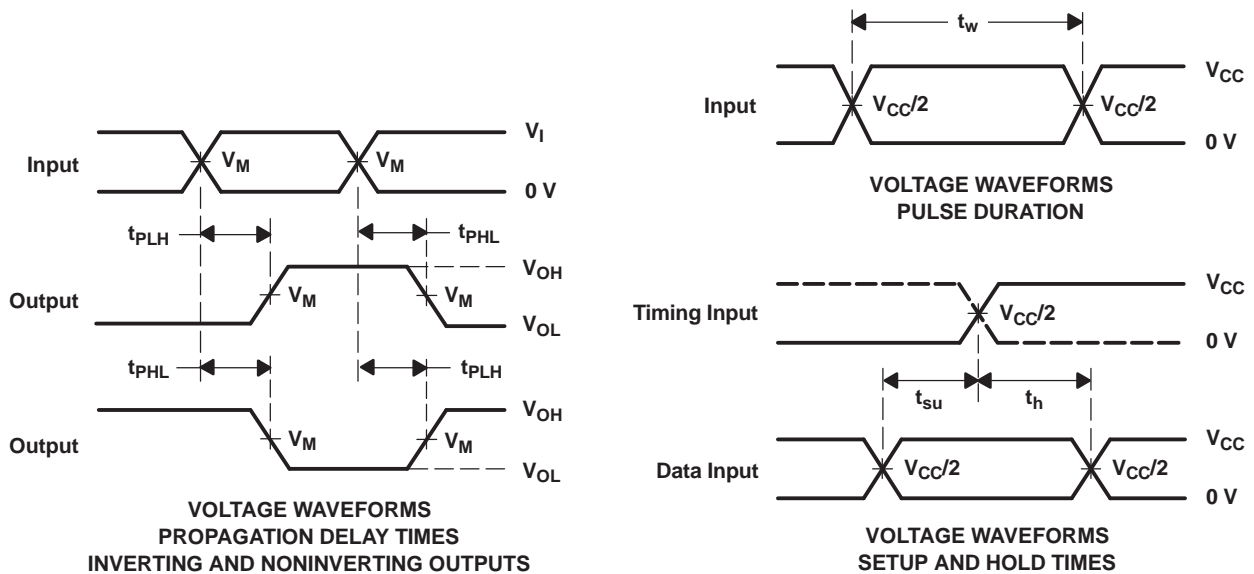
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$f = 10$ MHz	0.8 V	2.5	pF
		$1.2\text{ V} \pm 0.1\text{ V}$	2.5	
		$1.5\text{ V} \pm 0.1\text{ V}$	2.5	
		$1.8\text{ V} \pm 0.15\text{ V}$	2.5	
		$2.5\text{ V} \pm 0.2\text{ V}$	3	
		$3.3\text{ V} \pm 0.3\text{ V}$	3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

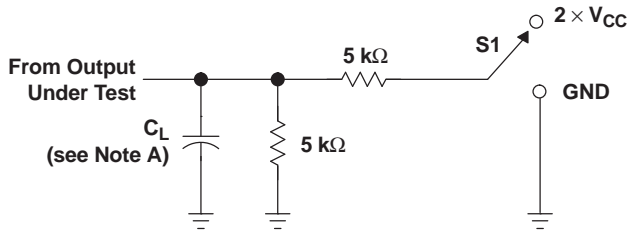
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V}$ $\pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

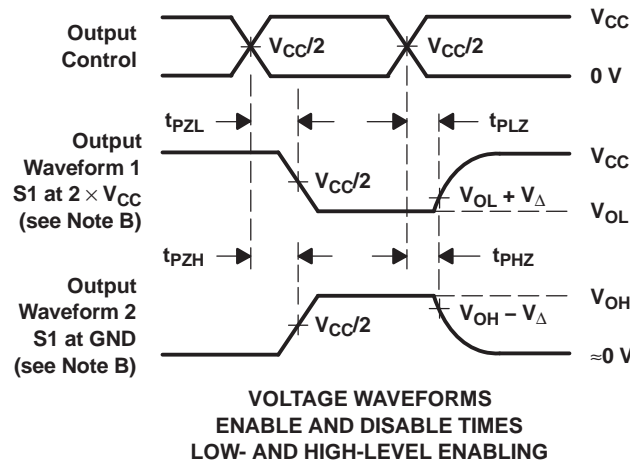
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t _{PLZ} /t _{PZL}	2 × V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP1G79DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G79YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G79DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74AUP1G79DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.66	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

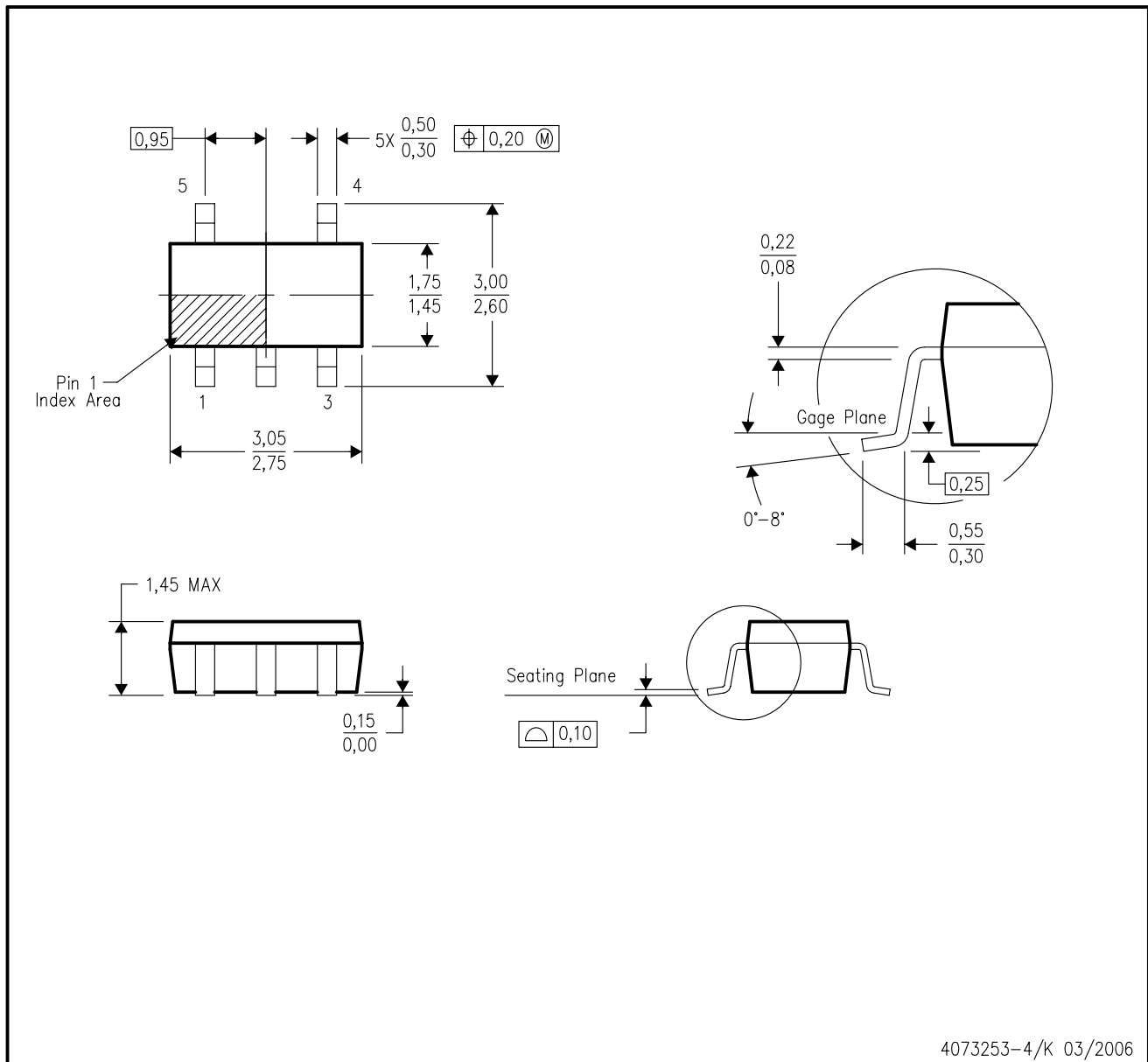


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G79DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G79DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G79DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G79DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

DBV (R-PDSO-G5)

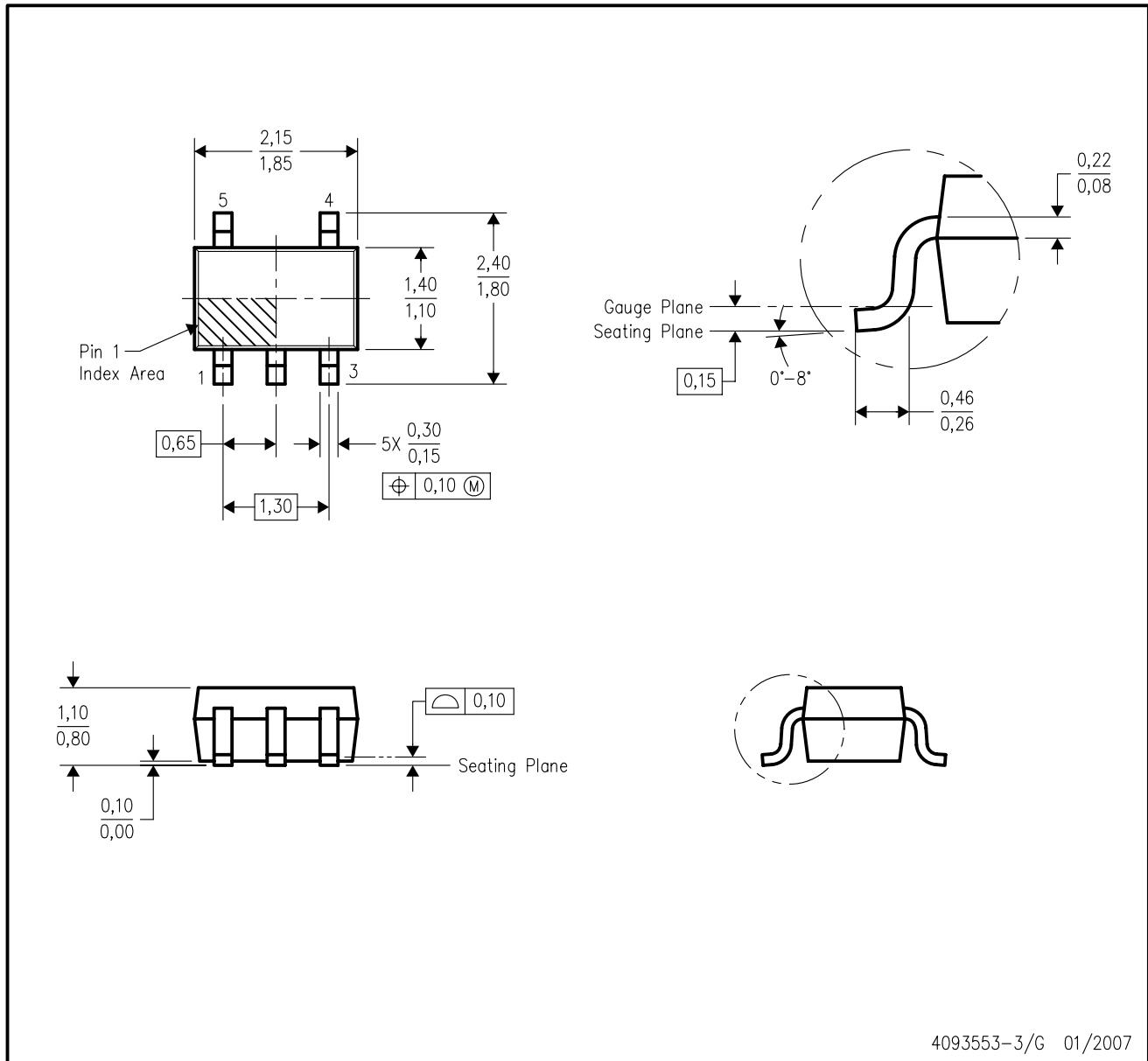
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



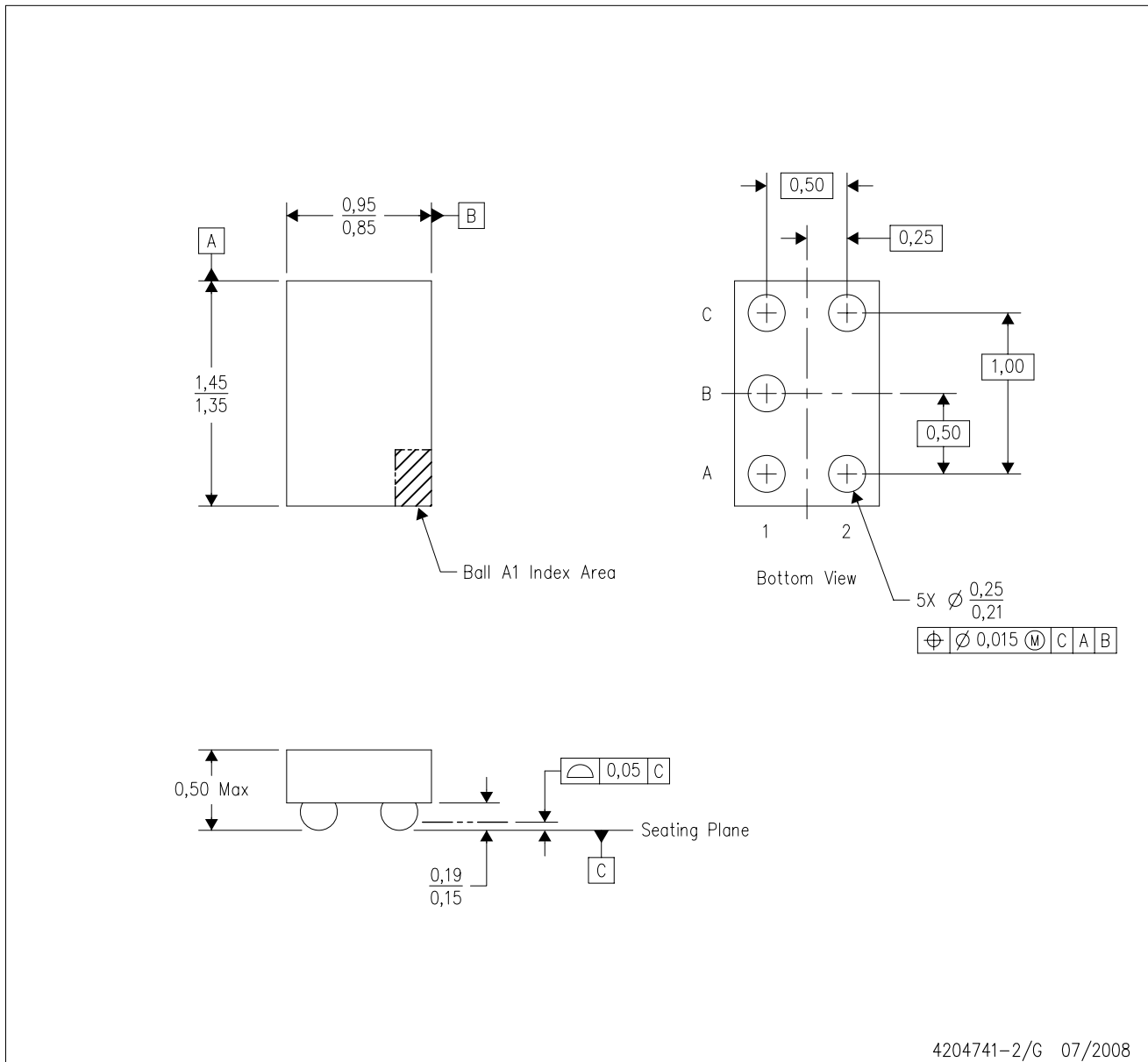
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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